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# Implementation of Transceiver in GMSK Communication Using Iterative Algorithm

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***Abstract:*** **The use of wireless products has been rapidly increasing their popularity in the last decades, similarly minimum shift keying (msk) is one of the most popular modulation methods in this wireless communication system .the technique for occupying less bandwidth and power for a given probability of error, Gaussian minimum shift keying (gmsk) modulation scheme is used in the project. the project involves the designs of communication system which is transceiver this transceiver system includes transmitter and receiver blocks. So that low power, high spectrum efficient communication system is implemented. Modulation is works an using frequency synthesizer (fs) such that system has reduced delay power efficiency, and area optimization characteristics on FPGA.**

***Keywords:*** **FS, CIC, MSK, GMSK, GAUSSIAN FILTER.**

## 1. INTRODUCTION

In wireless communication system, it must has the system design such that, which meet the delay reduction, area optimization and power efficiency, using available resources with the less cost, so can use fpga to implement the system design to meet all these criteria. Modulation and demodulation are the most important aspect in the communication, so have to choose an effective method to implement. one of the techniques for occupying less bandwidth and power, gaussian minimum shift keying (gmsk) modulation scheme [1] is used in the project and it also has advantages of being able to carry digital modulation while still using the spectrum efficiently and there is no sidebands extend outwards from the main carrier and hence there is no interference to other radio communications systems using nearby channels. gmsk is derived from continuous phase frequency shift keying method (cpfskm) by selecting the frequency deviation to be the minimum possible and filtering the baseband modulating signals with a gaussian filter. all this is to be done to minimize the spectrum width of the signal. to achieve all these criteria on communication system requires large recourses on fpga, to reduce the area on field programmable gate array (fpga), distributed algorithm or distributed arithmetic algorithm (da) is used. da is a computation algorithm that performs multiplication with look-up based scheme, which is inspired by the potential of the xilinx fpga look-up table architecture. da specifically targets the sum of products computation that covers many of the important dsp filtering and frequency transforming functions. so that the advantages gmsk modulation method can be utilized in a number of wireless communications applications such as gsm and edge technologies etc. the modules (transmitter and receiver) is describe using vhdl and implemented on the spartan 3e fpga.

There are only a few known implementations of this kind of systems on fpga [1] [2] [3] [4]. to make this design very useful for future developments, the entire system are developed with modular blocks interconnected [1], using input and output enable control signals. fig. 1.1 shows the transmitter block diagram, input is given to guassian filter which romoves noice and avoides interference with other signals. the output of the guassian filter is passed for modulation, discrete frequecny synthesizer (dfs) modulates the incoming binary data, two different carrier frequencies are generated for '0' and '1'. the generated carrier signal frequency is increased using cascade integrate combs (cic) filter, which acts as a upsampler in transmitter part to avoid aliasing effect. finally tansmitter part sends the signal to receiver.

## 2. SYSTEM DESIGN

GMSK digital modulation highly used in radio communication systems due to the advantages that it presents, one of these advantages is the spectrum efficiency provided by a gaussian filter. Modules (transmitter and receiver) are described on vhdl and implemented on the spartan 3e fpga. There are only a few known implementations of this kind of systems on

fpga [2] [3], making this design very useful for future developments. the entire system is developed with modular blocks interconnected [4], using input and output enable control signals, the number representation of the system uses a bit width of 8 which provides the necessary resolution for the system to work.

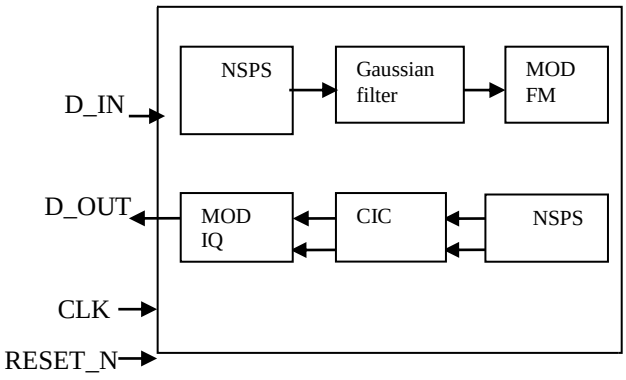


**Figure 2.1: Transmitter block diagram**

figure 2.1 shows the transmitter block diagram, on the transmitter the binary input data are presented with a 1 khz sample rate. the gaussian filter represents each input symbol with 8 new

samples in order to limit the band width (bw) of the signal. the fm (frequency modulation) modulator uses a 0 hz carrier. the cascade integrator combs (cic) filter used to increase the sample frequency. i/q (in-phase/quadrature) modulator translate input into signal spectrum, which is stored in the text file and then it is used as input for receiver.

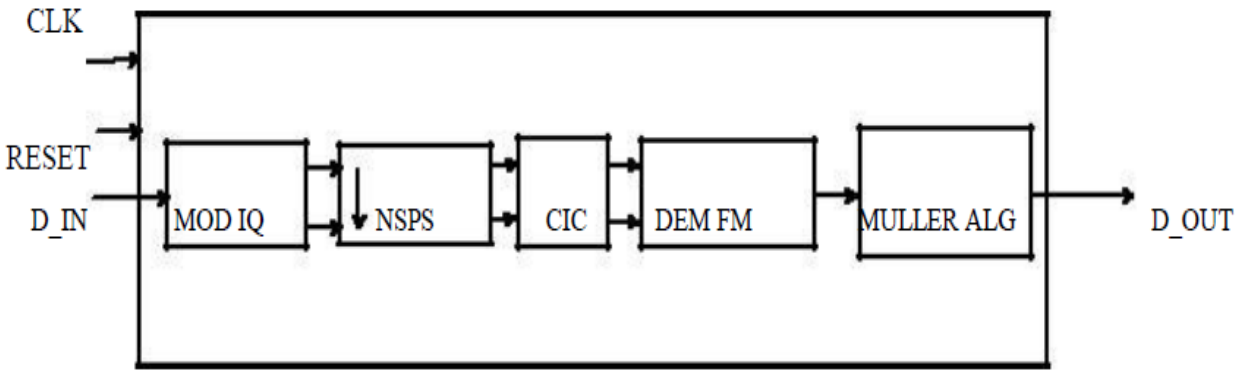


**Figure 2.2: Receiver block diagram**

figure 2.2 shows the block diagram of receiver, stored output of the transmitter in the text file is given as input to i/q demodulator, which translates the input spectrum into base band. the cic filter reduces the sample rate. finally from dem fm can obtain transmitted digital

data back.

## 3. MECHANISM OF DA

Consider the inner product of two *n* dimensional vectors a and x given in eqn. 3.1, where a is a constant vector, gaussian coefficients are considered, x is the input sample vector, and *y* is the result.

$$y = \sum_{k=1}^{K} A_k x_k \qquad -3.1$$

Let $x_K$ be represented as an n-bit scaled 2's complement number, such that $|x_K| < 1$ produces

$$x_K = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \qquad -3.2$$

Where $b_{kn}$ are the bits (0 or 1) of $x_K$, $b_{k0}$ is the sign bit. Substituting eqn. 3.2 into eqn. 3.1 yields

$$y = \sum_{k=1}^{K} A_k[-b_{k0} + \sum_{n=1}^{N-1} b_{kn}\, 2^{-n}]$$
$$y = -\sum_{k=1}^{K} A_k b_{k0} + \sum_{k=1}^{K}[\sum_{n=1}^{N-1} A_k b_{kn}]2^{-n} \qquad \text{-3.3}$$

Equation 3.3 represents the distributed arithmetic computation. the values of $b_{kn}$ are either 0 or 1, resulting in the bracketed term in eqn. 3.3 having $2^N$ possible values. Expanding and rearranging the eqn. 3.3 yields the following equation.

$$y = \begin{cases} -[b_{10}\,A_1 + b_{20}\,A_2 + - - - b_{k0}\,A_k] \\ +[b_{11}\,A_1 + b_{21}\,A_2 + - - - b_{k1}\,A_k]2^{-1} \\ +[b_{12}\,A_1 + b_{22}\,A_2 + - - - b_{k2}\,A_k]2^{-1} \\ - \\ - \\ - \\ - \\ +[b_{1(N-1)}\,A_1 + b_{2(N-1)}\,A_2 \pm - - - b_{k(N-1)}\,A_k]2^{-(N-1)} \end{cases} \qquad -3.4$$

since a is a constant vector, the bracketed term can be recomputed and stored in memory using either a lookup table (lut) or rom, hence the table called as distributed arithmetic lookup table (dalut). For each bit depth, *n*, the lookup table is then addressed using the individual bits of the input samples, $x_K$ which are typically stored in a shift register chain. Using this implementation, regardless of the lengths of the vectors a and x, the final result *y* is computed in *k* cycles.

## 4. IMPLEMENTATION RESULTS

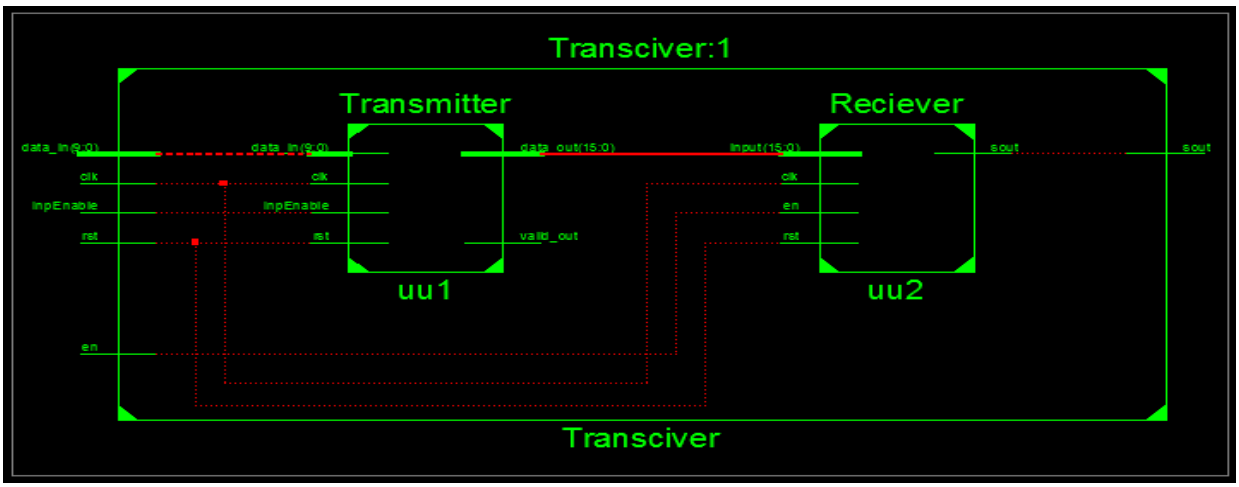


**Fig. 4.1 internal view of rtl schematic of transceiver**

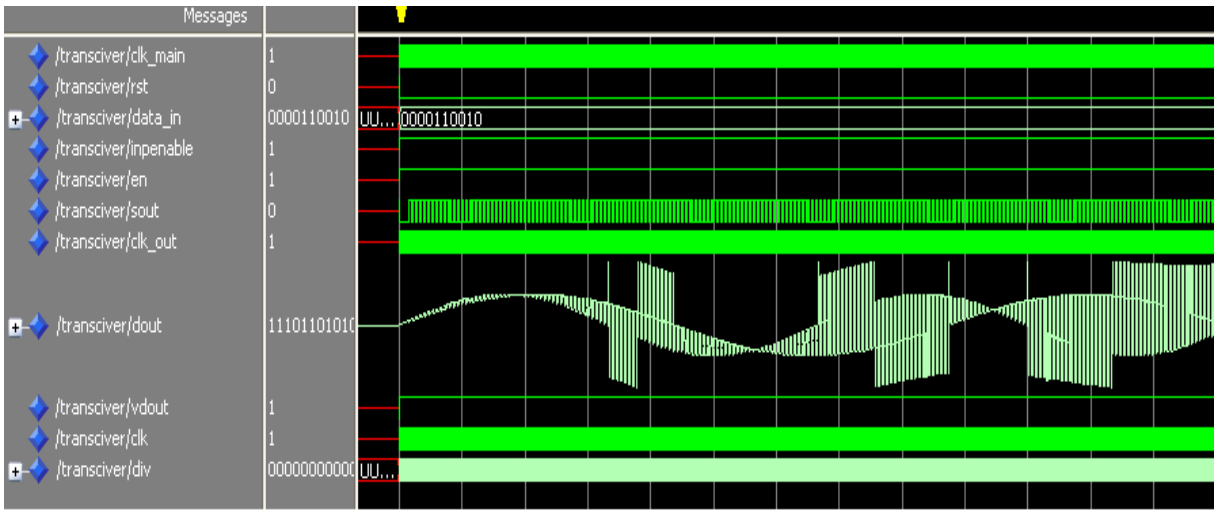


**Fig. 4.2 simulation result of transceiver**

Fig. 4.2 shows the simulation result of the whole transceiver. as clk is applied, reset, inpenable and en variables made high, then have to run system for few clock cycles. later reset has to make '0', after giving input bit to the variable data_in have to run_all and break. Finally the output will appear on the variable sout.

## 5. CONCLUSION

The transceiver part is designed and this communication system consists a transmitter and receiver parts the cic filters are allow low complexity computation due to their multiplier less structure. This requires huge number of multiplication and addition operation on fpga.

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